Digital Synchronous Demodulator for Measurement of Complex Amplitude Deviation

Yu. Artyukh, E. Boole, V. Vedin
Institute of Electronics and Computer Science, Dzerbenes st. 14, LV-1006 Riga, Latvia; phone: +371 7554500; e-mail: vedinv@edi.lv

Introduction

There are application cases where a sine-wave probing signal \( x_c(t) = A \sin(\omega t + \phi) \) is modulated in both amplitude and phase when it passes through some medium, resulting in the signal \( x(t) = A(t) \sin[\omega t + \phi(t)] \). Usually it is supposed that modulating frequencies are much lower than the frequency \( \omega \). Specifically, this is the case of bio-impedance measurement at frequencies over dozens of KHz under bio-modulation caused by heart beating and respiration [1].

To detect such modulation, one usually uses complex synchronous demodulation that can describe complex amplitude deviation as a function of time. In most cases the complex synchronous demodulation includes multiplying the signal \( x(t) \) by two conjugate reference signals \( \cos \omega c t \) and \( \sin \omega c t \), where \( \omega c \) is the central frequency of the signal \( x(t) \). Low-pass filtering of the multiplied signals gives two low-frequency signals that directly reflect complex amplitude deviation under some modulation process.

Basically the synchronous demodulation is performed using well-known analog techniques of frequency mixing and signal filtering. Below we will consider an approach to synchronous demodulation performed fully digitally by a specialised demodulator subsequently referred to as DM-processor.

Theory of DM-processor operation

Let’s suppose that the modulated signal \( x(t) \) has nearly constant values of peak amplitude \( A_i \) and phase \( \phi_i \) within some time interval from \( t_i \) to \( t_i + T_a \), where \( T_a \) is equal to a limited integer number of signal periods. This is just the case when the modulating frequencies are much lower than the frequency \( \omega \). Under this condition the complex amplitude of the signal \( x(t) \) at instant \( t_i \) can be defined by two Fourier coefficients:

\[
\begin{align*}
a(t_i) &= \frac{2}{T_a} \int_{t_i}^{t_i+T_a} x(t) \cos \omega c t \, dt; \\
b(t_i) &= \frac{2}{T_a} \int_{t_i}^{t_i+T_a} x(t) \sin \omega c t \, dt
\end{align*}
\]

(1)

Using these coefficients, the peak amplitude and phase of the signal \( x(t) \) at instant \( t_i \) can be further calculated as

\[
A_i = \sqrt{a^2(t_i) + b^2(t_i)} ;
\]

(2)

\[
\phi_i = -\arctg \frac{b(t_i)}{a(t_i)} .
\]

(3)

When the signal \( x(t) \) is presented in a form of periodic sequence of digital samples \( \{x(t_k)\} \) the expressions (1) take on the following forms:

\[
\begin{align*}
a(t_i) &= \frac{2}{N} \sum_{k=1}^{N} x(t_k) \cos \omega c t_k; \\
b(t_i) &= \frac{2}{N} \sum_{k=1}^{N} x(t_k) \sin \omega c t_k
\end{align*}
\]

(4)

Periodic calculation of the paired values \( \{a(t_i); b(t_i)\} \) results in presentation of complex amplitude deviation as function of discrete time.

However direct use of the expressions (4) for real-time calculation by DM-processor leads to high complexity of its implementation. Both continuous generation of digital sinusoidal functions and multiplication operations are too expensive for stand-alone implementation. To solve this problem DM-processor operation is based on the approach to digital spectral analysis considered in [2]. This approach suggests the use of binary (non-orthogonal) reference functions \( R_C \) and \( R_S \) instead of the above mentioned sinusoidal ones. These binary functions take the values “1” or “−1” depending on the sign of corresponding sinusoidal functions in (4). Thereby the calculations posed by the expressions (4) can be simplified down to accumulation of digital signal samples under real-time control for the sign of each sample being accumulated. Such control is performed according to the current values of continuously generated binary functions \( R_C \) and \( R_S \).

Evidently this results in considerable complexity reduction of DM-processor design. The data accumulation can be implemented by relatively simple logic circuits and provide higher operation speed comparing to microprocessors usually used for similar purposes.
Let’s note that generally such approach to estimation of Fourier coefficients needs additional correction of initial estimates obtained by the mentioned short-cut calculation. However, when the signal $x(t)$ is narrow-band, such correction is not essential and may be omitted. But in this case possible uneven harmonics of the input signal (e.g., caused by its non-linear distortions in a front-end circuit) will not be suppressed, which causes specific errors of complex amplitude estimation.

The chip contains two identical 24-bit data accumulators and multiplexer to direct data from both accumulators into FIFO memory (see Fig.1). The reference signals $R_C$ and $R_S$, which are continuously generated by an additional PLD chip, specify the sign of accumulated data during the preset number of these periods.

**Fig. 1. Schematic block diagram of DM-processor**

**DM-processor design**

DM-processor is designed according to the above principles of operation as a stand-alone peripheral device interfacing with a host PC via its parallel port (Fig. 1).

DM-processor receives input analog signal, estimates the values $\{a(t_i); b(t_i)\}$ for some specified part of this signal under either internal (periodic) or external triggering, and saves the measurement results in FIFO. These data are available for reading by PC at any instant. DM-processor, in interaction with PC, can support continuous (gapless) measurement during practically unlimited time. Before performing the measurements the PC presets all necessary parameters for DM-processor (value of the frequency $\omega_C$, number of processed periods, triggering mode etc).

DM-processor contains four basic functional blocks: analog-to-digital converter (ADC), processing block, FIFO and reference signal generator. Operation of all mentioned blocks is clocked by 10 MHz master clock.

An input analog signal is continuously converted at 10 MHz sampling rate to a periodic sequence of 12-bit samples by the ADC from “Burr-Brown” (ADS801). This sampling rate provides adequate oversampling ratio for input signal frequency up to 150 KHz. The ADS801 integral linearity is specified to be not more than ±1.7 bits and spurious-free dynamic range about -75 dBFS that is limited mainly by third spurious harmonic. This is enough to achieve relative precision better than 0.1% for estimation of Fourier coefficients directly by the DM-processor without additional corrections.

The on-chip control unit defines the time intervals for data accumulation (alternatively 2, 4, 8 or 16 periods), manages FIFO data flow, and supports the PC interface. The FIFO saves paired values $\{a(t_i); b(t_i)\}$ to be read by PC. Each pair (or readout) is presented in FIFO as a 48-bit data block; totally it can accumulate up to 10K of such data blocks.

A crucial part of the synchronous demodulation is the generating reference signals with exactly the same frequency as the central frequency $\omega_C$ of input signal. It is supposed that the probing signal will be formed directly from one of two square-wave reference signals by its low-pass filtering. Such signals are synthesized by the digital frequency dividers implemented within separate PLD chip. By the design requirement the nominal frequency of the reference signals is about 100 KHz although available frequency range is wider: 50 to 150 KHz.

Pilot version of the DM-processor has been designed as a single board (Fig. 2) that is adapted to embedding in complex system such as multi-channel bio-impedance analyser.

**Fig. 2. Design of the DM-processor**
Correspondingly the DM-processor also offers several ancillary signals to support coordinated interaction with other functional components (such as analog signal multiplexers) of the bio-impedance analyser.

Note that the design was intended mainly for feasibility studies and does not claim to be the best solution in terms of functionality, compactness, etc. If desired, similar design can be more closely adapted to the specific application.

Evaluation of the DM-processor performance

**Experimental set-up.** As the DM-processor is able to operate only in interaction with PC, an application program has been developed for that. This program can be used both directly for some common-used applications and for creating other specific programs on its basis.

The program provides flexible control of DM-processor operation, continuous data reading and calculation of both peak amplitude and phase readouts according to expressions (2-3). These values are displayed in forms of phase and amplitude deviation as a function of time. The program is written on C in LabWindow/CVI that provides a human-engineered Graphic User Interface (GUI) and many useful facilities to display the results in graphic form. As the test signal source, the standard signal generator SME 03 from “ROHDE&SCHWARZ” has been used. It provides high-purity test signal and different kinds of its modulation needed for the tests.

For all below considered tests the preset reference signal frequency was 96.1538 KHz; input signal was measured under periodic internal triggering every 0.1761 ms during 16 periods of the reference signal. Such measurement rate (5.678 KSPS) allows detecting the modulating process at frequencies up to 2.8 KHz. The program provides displaying of 1000 sequential readouts in scrolling mode which corresponds to the length of visible time window 0.1761 s.

**Precision of peak amplitude measurement.** When the ADC produces some non-linear distortions of input signal, the peak amplitude may be measured with some systematic error depending on the phase shift between input signal and reference signal. Although such error in principle can be corrected, it is of interest to specify its value to estimate necessity of such corrections for the specific application.

The observed noise floor corresponds to the RMS jitter of peak amplitude measurement of about 10-15 µV. Seeing that the input signal full range is ±1V, under our
test conditions such jitter corresponds to the resolution of peak amplitude measurement about 16-17 effective bits. Note that generally the resolution of peak amplitude measurement directly depends on the duration of single measurement predetermined by the preset number of the reference signal periods.

As for the initial phase estimation, its available resolution significantly depends on the amplitude of input signal. For relatively large input signals (peak amplitude >100 mV) the RMS resolution is typically about 0.001 of radian, but for small input signal (peak amplitude <10 mV) it can be in many times worse.

**Measurement rate.** Under cyclical operation the DM-processor can provide up to 10,000 readouts at measurement rate up to 50 KHz in each cycle using internal FIFO for data buffering. However, for continuous (gapless) measurement the maximum measurement rate is limited by the available speed of data reading by PC. Additionally it should be taken into account that data processing and displaying can additionally limit the measurement rate. Running our program on Pentium III (1.6 GHz) gave the maximum rate of continuous measurement of about 9 KHz.

1. **Considered approach to synchronous digital demodulation provides both simplicity of implementation and good performance.** As the experimental results indicate, it can support the resolution of peak amplitude measurement at least 16-17 effective bits in KHz frequency range of complex modulation. As for maximum measurement rate, it is mainly limited by available speed of PC data transfer.

2. **Described design of the DM-processor was oriented mainly to bio-impedance analysis.** However the similar principles of digital demodulation may be used for various designs adapted to specific applications.

**References**


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Considered demodulator uses periodic rectangular functions instead of conventional sinusoidal ones for calculation of Fourier coefficients defining complex amplitude. This allows considerable simplifying the demodulator design and increasing its operation speed. Specifically, the demodulator provides periodic measurement of phase and peak amplitude of narrowband signal in KHz frequency band of its complex modulation with effective amplitude resolution about 16-17 bits. The demodulator is mainly oriented to applications related to bio-impedance analysis under natural bio-modulation. Ill. 5, bibl. 2 (in English; summaries in English, Russian and Lithuanian).


Рассмотренный демодулятор использует периодические прямоугольные функции вместо обычных синусоидальных для вычисления коэффициентов Фурье, определяющих комплексную амплитуду. Это позволяет существенно упростить реализацию демодулятора и повышить его быстродействие. В частности, демодулятор обеспечивает периодическое измерение фазы и пиковой амплитуды узкополосного сигнала в полосе частот его комплексной модуляции до нескольких КГц с эффективным разрешением по амплитуде 16–17 бит. Демодулятор ориентирован главным образом на применения, связанные с анализом био-импеданса в условиях его естественной био-модуляции. Ил. 5, библ. 2 (на английском, русском и литовском яз.).


Analizuojamas modulatoriumis Fūryje koeficientams, nusakantiemis kompleksinei amplitūde, apskaičiuoti vietoje įprastų sinusinių funkcijų naudoja periodines stačiakampes funkcijas. Tai leidžia iš esmės supaprastinti demodulatoriaus struktūrą ir padidinti jo greitaveiką. Demodulatoriumi atliekami periodiniai fazės ir pikinės siaurajuosčio signalo amplitudės matavimai kompleksinės moduliacijos dažnių juostose iki keleto kHz, esant efektyviam amplitudės 16–17 bitų skirtumui gebai. Demodulatoriui naudojamas bioimpedansio analizei, esant natūralioms biomoduliacijos sąlygomis. II. 5, bibl. 2 (anglų kalba; santraukos anglų, rusų ir lietuvių k.).